REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on July 9, 2003, and the references cited therewith.

Claims 11, 24, 28, 38, and 40 are amended, no claims are canceled, and no claims are added. As a result, claims 11, 13, 14, 24-28, 32, and 38-43 are now pending in the application.

§102/§103 Rejection of the Claims

Claims 11, 14, 24, 25, 28, 32, 38, 40, and 41 were rejected under 35 USC § 102(b) as being anticipated by, or in the alternative under 35 USC § 103(a) as being obvious over Selvakumar et al. (U.S. Patent No.5,426,069). Claims 11, 14, 24, 25, 28, 32, 38, 40, and 41 were rejected under 35 USC § 102(b) as being anticipated by, or in the alternative under 35 USC § 103(a) as being obvious over Nakagawa (U.S. Patent No. 5,272,365).

The Office Action states that claims 11, 14, 24, 25, 28, 32, 38, 40, and 41 are product by process claims. Applicant has amended claims 11, 24, 28, 38, and 40, and respectfully submits that only product limitations are now found in these claims.

The Office Action states on page 21, fourth paragraph, that "Applicant has failed to meet the burden clearly set forth in the Office Action mailed January 9, 2003 (i.e. the burden to come forward with evidence establishing an unobvious difference between the claimed product and the prior art products as per MPEP §2113)."

Applicant respectfully submits that a *prima facie* case of anticipation or obviousness must first be established by the Patent Office before evidence to rebut an established *prima facie* case is required. *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). In order to establish a *prima facie* case, the reference or combined references must teach or suggest all the claim elements. M.P.E.P. § 2142 (citing *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed.Cir. 1991)).

The rejections state that the $Si_{1-x}Ge_x/SiO_2$ region of Selvakumar or alternatively Nakagawa "forms a continuous $Si_{1-x}Ge_x/SiO_2$ gate oxide interface wherein no germanium oxide is present at the $Si_{1-x}Ge_x/SiO_2$ gate oxide interface. Applicant respectfully traverses the assertion that Selvakumar or Nakagawa show a device that includes both a continuous $Si_{1-x}Ge_x/SiO_2$ gate

oxide interface; and a gate oxide interface where no germanium oxide is present at the $Si_{1-x}Ge_x/SiO_2$ gate oxide interface. While both Selvakumar and Nakagawa appear to show gate oxides that include silicon oxide, Applicant is unable to find sufficient detailed description of the interface as claimed in the present application in either Selvakumar or Nakagawa to establish a *prima facie* case of obviousness. Selvakumar in column 4, lines 18-19 discuss a silicon germanium region surrounded by silicon, thus a continuous $Si_{1-x}Ge_x/SiO_2$ gate oxide interface is not shown. Nakagawa in column 5, lines 19-30 discuss a gate insulation layer 18, but the purity (for example germanium oxide content) is not discussed.

Further, in support of Applicant's position, Applicant respectfully submits that the processes used in Selvakumar and in Nakagawa cannot produce a device that includes both a continuous $Si_{1-x}Ge_x/SiO_2$ gate oxide interface; and a gate oxide interface where no germanium oxide is present at the $Si_{1-x}Ge_x/SiO_2$ gate oxide interface.

The process of forming the gate oxide in Selvakumar is described in Col. 3, lines 40-68, and in Col. 4, lines 1-3. The description in Selvakumar appears to include first implanting germanium through an exposed window (Col. 3, lines 41-44), then forming a dry gate oxide (Col 3, lines 45-48). Forming the dry oxide is further described as being performed at 1100° C for 50 minutes in dry oxygen and a 20 minute nitrogen anneal. The process of forming the gate oxide in Nakagawa is described in Col. 5, lines 23-28. The gate oxide 18 of Nakagawa appears to be formed subsequent to the implantation step by a thermal oxidation process.

Applicant submits that, depending on the process conditions of the ion implantation, the ion implantation process either leaves the Ge atoms exposed at the surface to be oxidized, or it buries the Ge atoms in the substrate beneath the surface to be oxidized. The Selvakumar reference appears silent as to depth of implanted Ge atoms. Applicant submits that in either case, the product resulting from the described process as taught by Selvakumar does not produce a $Si_{1-x}Ge_x$ region with both: a continuous $Si_{1-x}Ge_x/SiO_2$ gate oxide interface; and no germanium oxide present at the $Si_{1-x}Ge_x/SiO_2$ interface. Nakagawa appears to describe an embodiment in Figure 1 where the SiGe region is buried beneath an intermediate silicon layer, and an embodiment in Figure 3 where the SiGe region includes exposed Ge atoms prior to oxidation to form the gate oxide.

If the implanted Ge atoms are buried, then by definition, an intermediate silicon layer exists between the channel surface to be oxidized and the implanted Ge atoms. A continuous $Si_{1-x}Ge_x/SiO_2$ gate oxide interface does not exist due to the intermediate layer of silicon. If the implanted Ge atoms are exposed on the surface to be oxidized, Applicant submits that one skilled in the art will recognize that using the subsequent oxidation process of Selvakumar or Nakagawa as described above, germanium oxide will necessarily be created at the $Si_{1-x}Ge_x/SiO_2$ gate oxide interface. Germanium oxides are undesirable because they are not stable, as discussed on page 2, lines 16-19 of Applicant's specification. Neither the Selvakumar reference, nor the Nakagawa reference appear to recognize or address the negative aspects of germanium oxides.

In contrast, devices as claimed by Applicant, and products produced by the process claimed by Applicant include a continuous $Si_{1-x}Ge_x/SiO_2$ gate oxide interface wherein no germanium oxide is present at the $Si_{1-x}Ge_x/SiO_2$ gate oxide interface. Applicant's unique process implants the germanium after the gate oxide has been formed. The implant of germanium atoms in Applicant's process is directed through the gate oxide, and forms a $Si_{1-x}Ge_x$ channel region and a continuous $Si_{1-x}Ge_x/SiO_2$ gate oxide interface. No oxidation steps are performed in Applicant's process subsequent to the germanium being introduced to the channel region.

The process of Applicant's invention therefore leads to a unique structure implied by the process recited in the claims. No germanium oxide will be formed at the $Si_{1-x}Ge_x/SiO_2$ gate oxide interface formed in Applicant's invention because the germanium in Applicant's process is never exposed to an oxidation step. As noted above, germanium oxides are undesirable because they are not stable, as discussed on page 2, lines 16-19 of Applicant's specification.

Although not directly cited in a 35 USC § 102 or § 103 rejection, the pending office action refers to the Chan reference (U.S. Pat. No. 5,801,396). The Office Action points to column 7, lines 16-18 of Chan where it states that "SiGe alloys at low concentrations provide grown oxides which are reasonably close in quality to those grown on pure Si."

Chan appears to teach "inverted transistors" (col. 3, line 47). Applicant is unable to find teaching to any embodiments other than inverted transistors. In the inverted design of Chan, the channel region is grown on the gate oxide. The channel region of Chan is therefore located *over* the gate oxide.

In contrast, devices as claimed by Applicant, and products produced by the process claimed by Applicant include a $Si_{1-x}Ge_x$ channel region, having a germanium molar fraction x, located **underneath** the SiO_2 gate oxide and between the source/drain regions, wherein x is less than or equal to 0.6, and wherein the $Si_{1-x}Ge_x$ channel region forms a continuous $Si_{1-x}Ge_x/SiO_2$ gate oxide interface wherein no germanium oxide is present at the $Si_{1-x}Ge_x/SiO_2$ gate oxide interface.

The quote from Chan cited in the present Office Action appears to discuss a motivation of the Chan reference for using an inverted transistor design. The quote from column 7, lines 16-25 appears to merely discuss "grown oxides." No mention is made as to a presence or lack of germanium oxide in a "grown oxide."

Because the Selvakumar and the Nakagawa reference each taken alone do not show every element of Applicant's independent claims, a 35 USC § 102(b) rejection is not supported. Further, applicant submits that for the reasons stated above, an alternative 35 USC § 103(a) rejection is not supported by the cited single references when presumably combined with general knowledge. Reconsideration and withdrawal of the rejections is respectfully requested with respect to Applicant's independent claims 11, 24, 25, 28, 38, 40, and 41. Additionally, reconsideration and withdrawal of the rejection is respectfully requested with respect to the remaining claims that depend therefrom as depending on allowable base claims.

§103 Rejection of the Claims

Claims 13, 26, 27, 39, 42, and 43 were rejected under 35 USC § 103(a) as being unpatentable over Selvakumar et al. together with Crabbe' et al. (U.S. Patent No. 5,821,577). Claims 13, 26, 27, 39, 42, and 43 were rejected under 35 USC § 103(a) as being unpatentable over Nakagawa together with Crabbe' et al.

Applicant respectfully submits that the Crabbe reference fails to cure the deficiencies of Selvakumar and Nakagawa as discussed in arguments above. Because the cited references, either alone or in combination, do not show every element of Applicant's claims 13, 26, 27, 39, 42, and 43, a 35 USC § 103(a) rejection is not supported by the references. Reconsideration and withdrawal of the rejection is respectfully requested.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 373-6944 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, P.O.Box 1450, Alexandria, VA 22313-1450, on this 9 day of October, 2003.

Tina Kohat
Name

Signature